SEMICONDUCTOR INDUSTRY ASSOCIATION

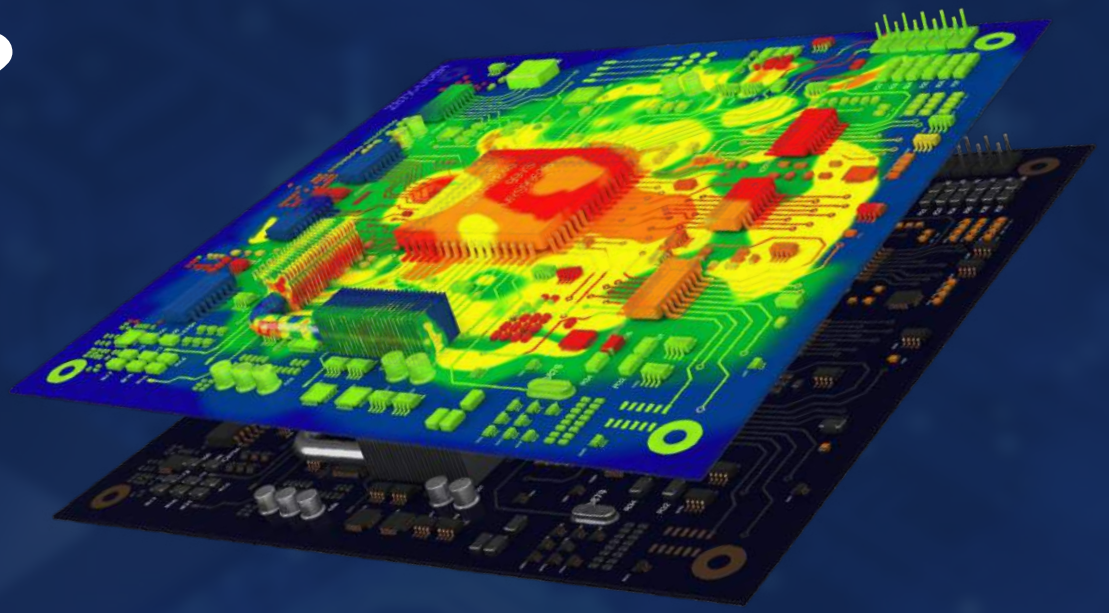
INNOVATION & COMPETITIVENESS: U.S. Chip Design Leadership in the 21st Century

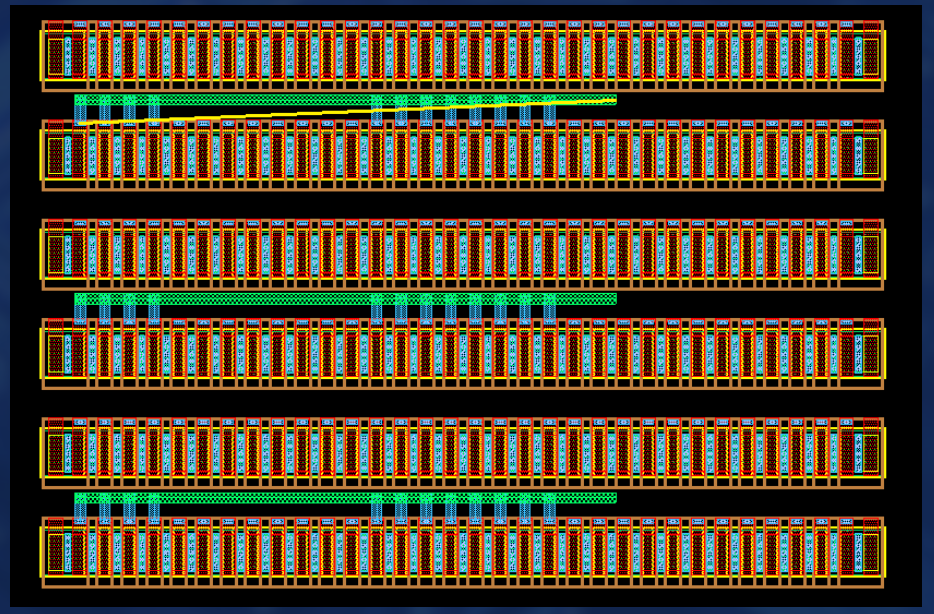
June 27, 2023

WHAT IS CHIP DESIGN?

- The process of laying out the “architecture” and developing the system of a chip to achieve a specific function or application for a product

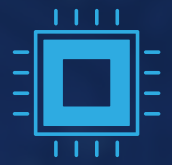
- An R&D, engineering, IP, talent, time, and cost intensive process of mapping billions of transistors and electronic components to relay instructions to the device that enable today’s digital world





FOUR MAJOR STAGES OF CHIP DESIGN






1

Product definition and specification

Product management, system architecture, and customer define initial product requirements

2

Architecture/ system design

System architects define block-level architecture for the design and may leverage previous IP (such as a chiplet)

3

Integrated circuit design

Multidisciplinary effort

- Logic: Initial analog and digital design
- Circuit: Digital synthesis and design for test
- Layout: Routing and mask generation

Packaging design

Design for advanced packaging functions

Verification

Verification engineers verify design functionality and timing through simulation

4

Post-silicon validation

Validation engineers validate physical device functionality across extreme working conditions

Sources: White House 100 Day Supply Chain Review Report; BCG analysis.

BUSINESS MODELS INVOLVING CHIP DESIGN

Fabless

Focus on chip design and partner with a foundry for fabrication

Integrated Device Manufacturer (IDM)

Design *and* manufacture their own chips

Original Equipment Manufacturer (OEM)

Design chips for their own end products (phones, cars, data centers, etc.) and outsource fabrication.

Electronic Design Automation & IP

Firms that provide software and hardware used for the complex modeling needed in chip design, as well as some application specific design services

CHIP DESIGN IN THE SUPPLY CHAIN

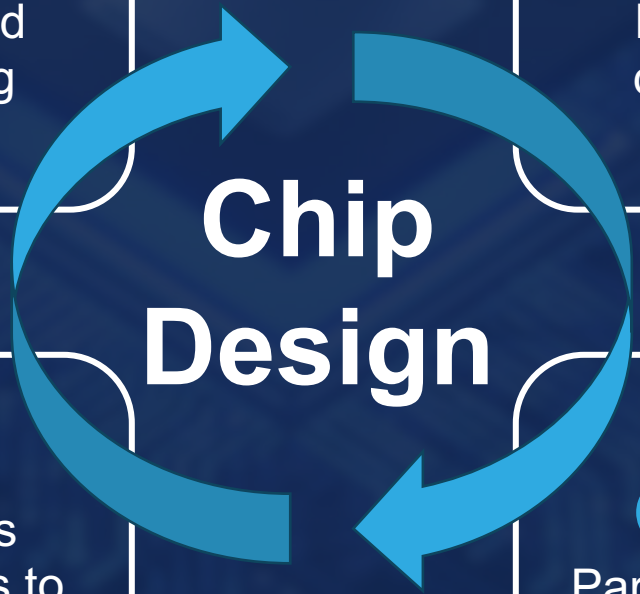
Companies that design chips have their fingerprints on the whole ecosystem

IP & EDA

Develop needed architectures and simulation and complex modeling tools to enable new designs.

Equipment Makers

Ensure design compatibility and develop new equipment to meet design technology needs



Customers

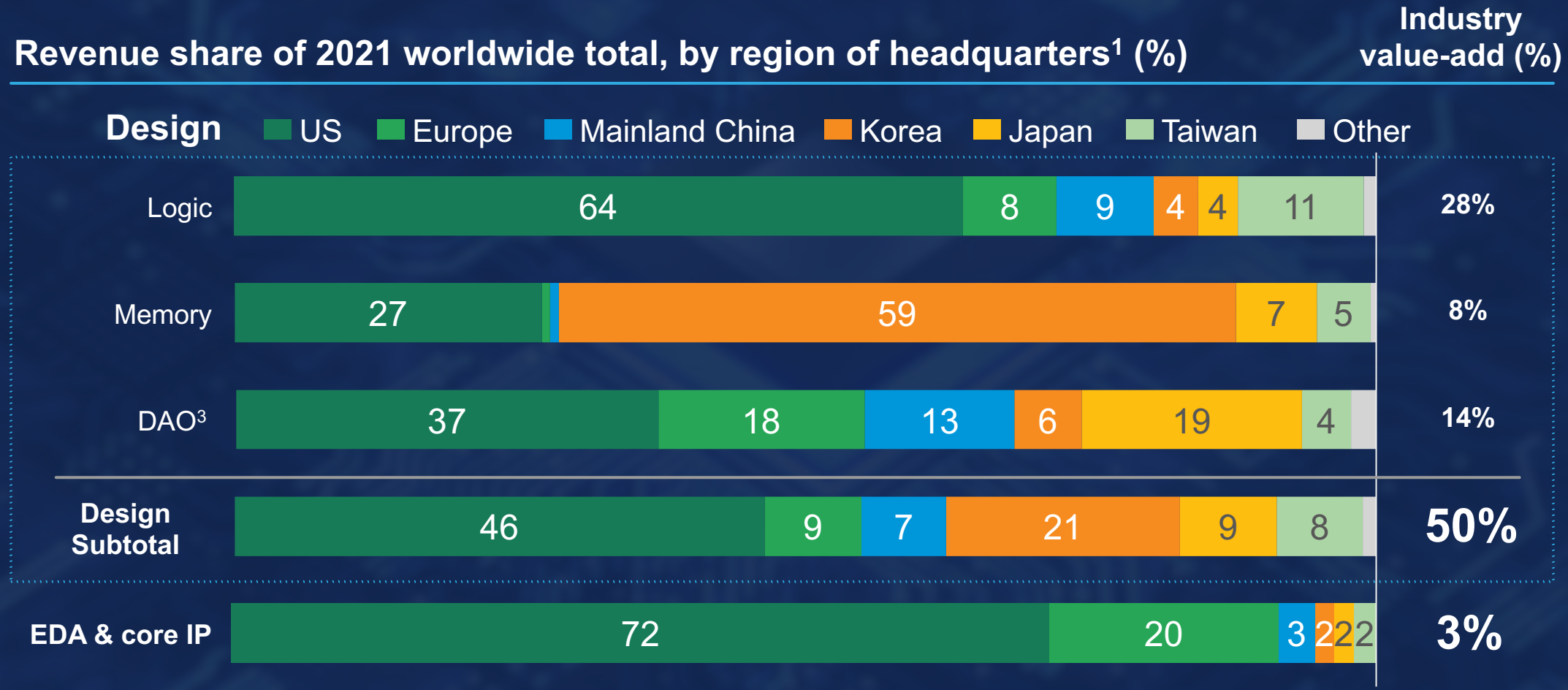
Collaborate on designing-in chips for products or specific applications to meet functionality and performance requirements

Manufacturers

(foundries, OSATs, in-house)

Partner to achieve technical feasibility for fabrication/packaging, including to develop new process technologies

THE U.S. IS THE LONGSTANDING LEADER IN SEMICONDUCTOR DESIGN REVENUE



Source: Capital IQ, SIA Factbook 2022, BCG analysis
Note: DAO = discrete, analog, and other; EDA = electronic design automation; IP = intellectual property. Because of rounding, not all bar segment totals add up to 100%.
[1] The regional breakdown is based on company revenues and headquarters location. Design revenues are based on fabless companies and estimated share of IDM revenues attributable to design. [2] R&D Intensity, measured as R&D divided by revenue [3] Discrete, analog, optoelectronics, sensors, and others.

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IMPORTANCE OF U.S. DESIGN LEADERSHIP


AI


Energy


Defense


Healthcare


Agriculture


5G/6G


Transportation

Design Leadership *is* Technology Leadership

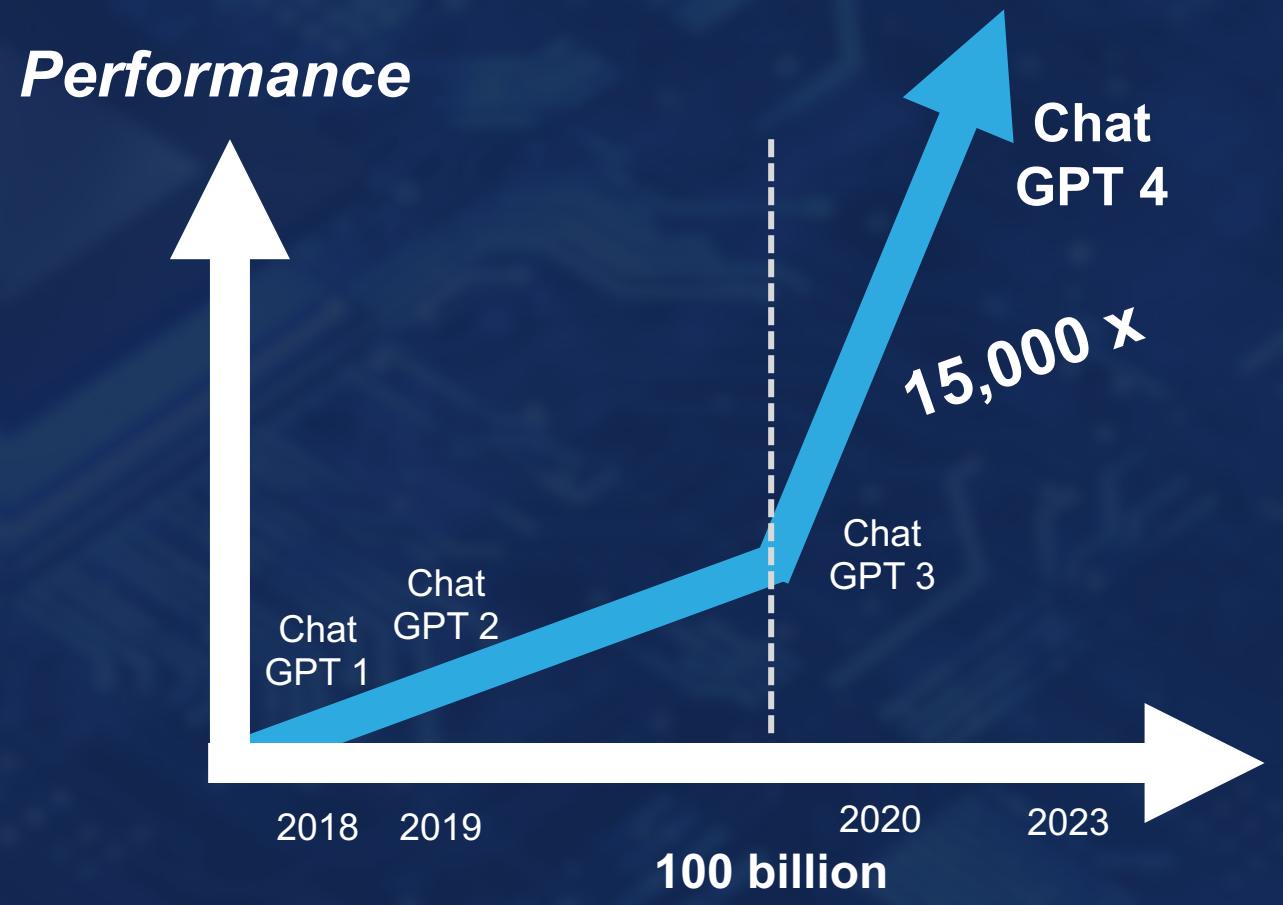
- Breakthroughs in semiconductor-enabled technologies
- "First mover" advantage in countless industries
- Global reliance on U.S.-designed chips
- Cycles of innovation in semiconductor manufacturing and equipment
- Software, services, and products based on U.S. design technology
- Influence in setting standards and technical "rules"

DESIGN ENABLING AI

Advances in semiconductor technology underpin breakthroughs in AI hardware, software, and services

AI chips expected to experience **228% growth**[1] from 2021-2027

Semiconductor innovation needed for **collecting, storing, and processing** exponentially increasing amounts of information



[1] Gartner

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DESIGN ENABLING ENERGY EFFICIENCY

As technology consumes more information, chips need to be designed to compute more efficiently

Data centers

Personal electronics

Networks

Cloud computing

Frontier Supercomputer at Oak Ridge National Labs in Tennessee

U.S. DEPARTMENT OF ENERGY

Energy Efficiency Scaling for 2 Decades
DOE initiative to develop semiconductor energy efficiency roadmap

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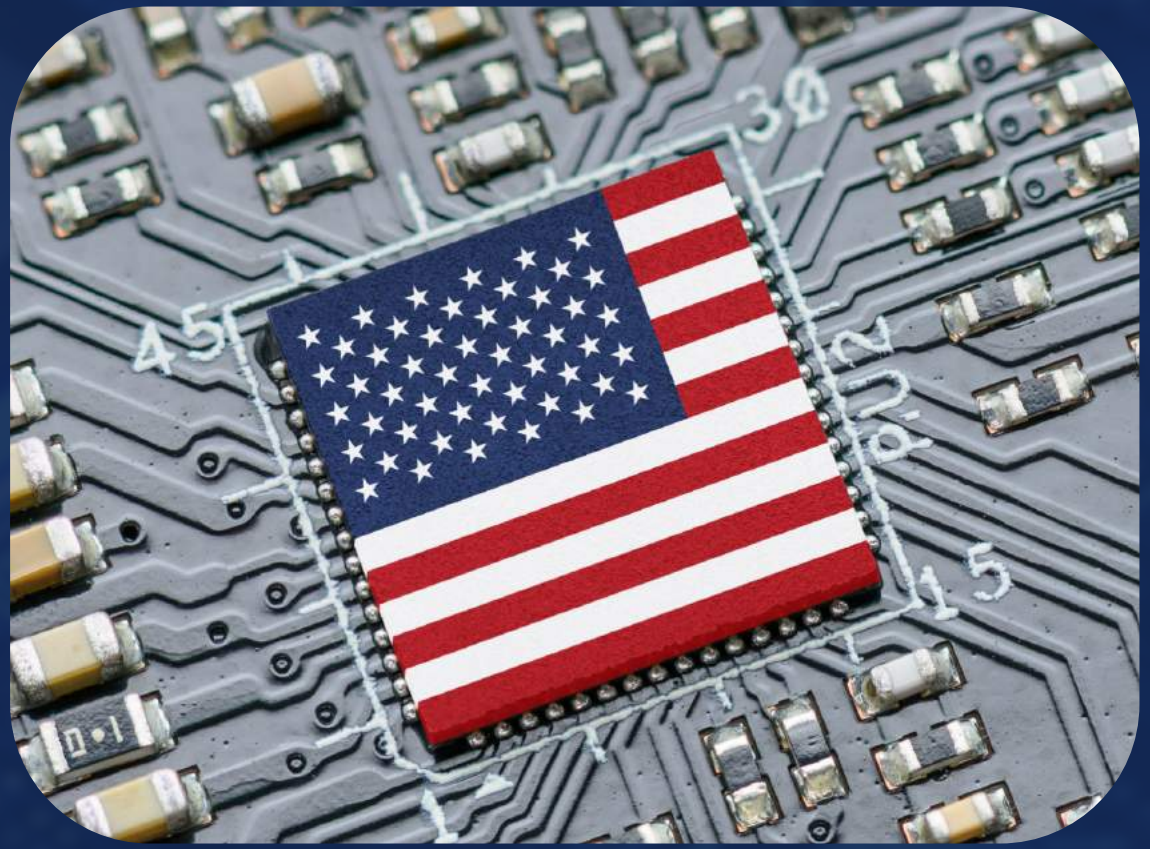
DESIGN ENABLING NATIONAL SECURITY

Semiconductor applications for defense systems; Design with security for commercial use

Innovation for the defense industrial base – warfighter system performance, weapons, secure communications, aircraft, etc.

Anti-tampering architectures for tampering detection, resistance, and evidence

Protection and control of **intellectual property**

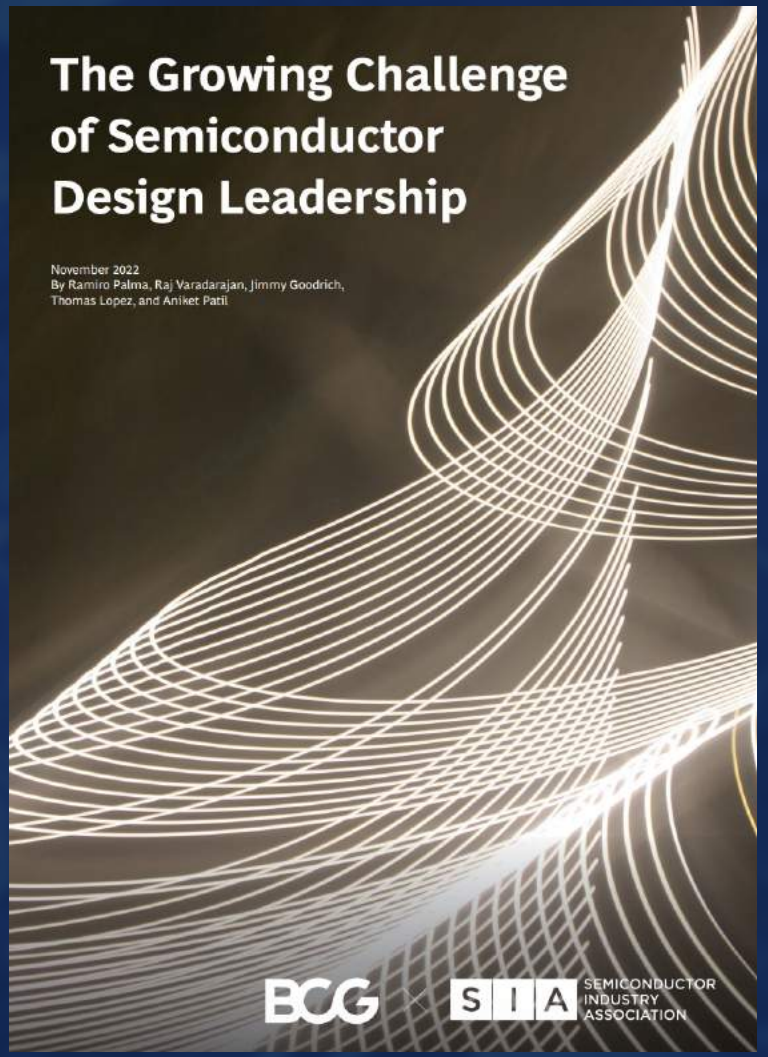


CHALLENGES FACING U.S. CHIP DESIGN LEADERSHIP

1. Exponentially increasing costs of design

2. Challenges from global competitors

3. Access to high-skilled talent



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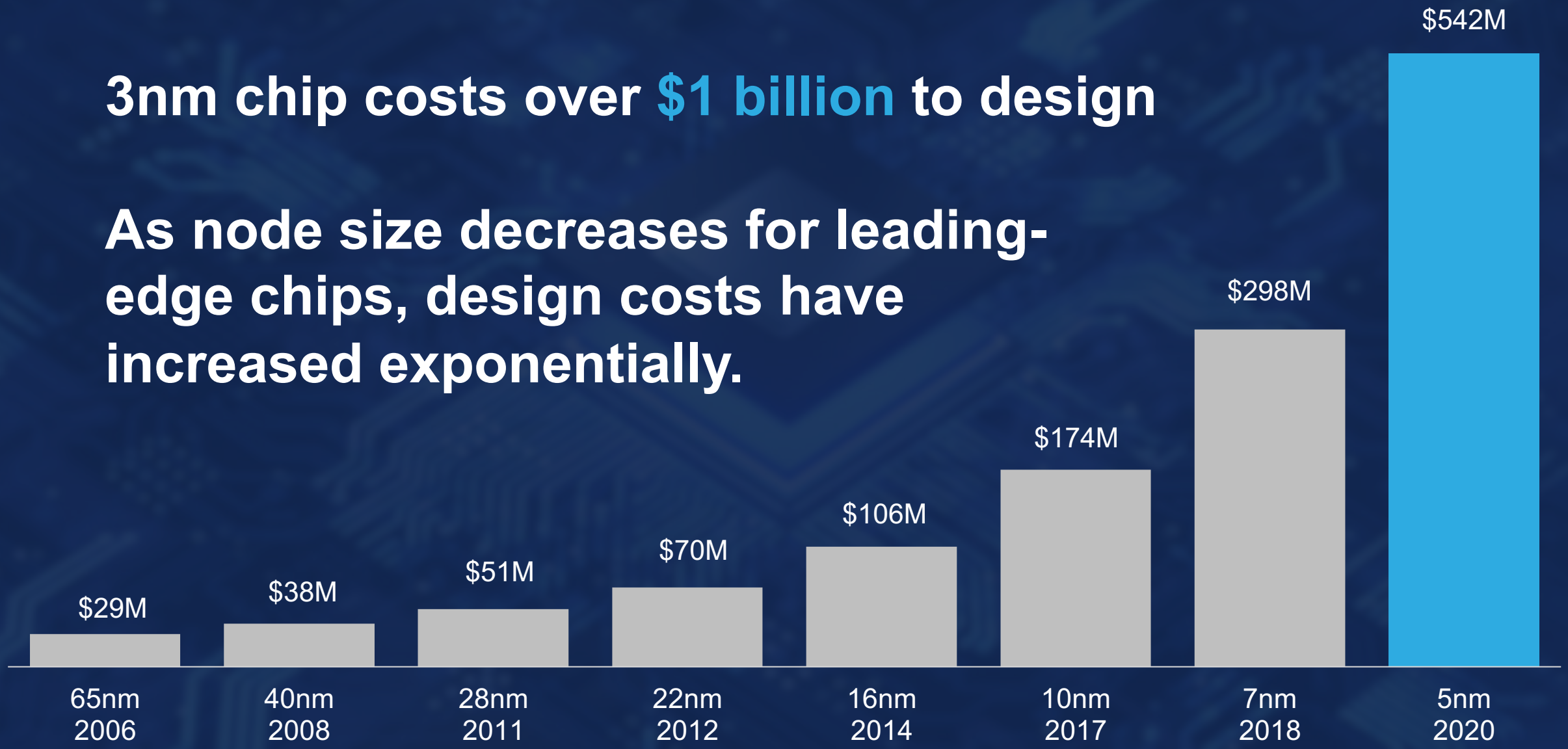
DESIGN COSTS ARE RISING

3nm chip costs over $1 billion to design

As node size decreases for leading-edge chips, design costs have increased exponentially.



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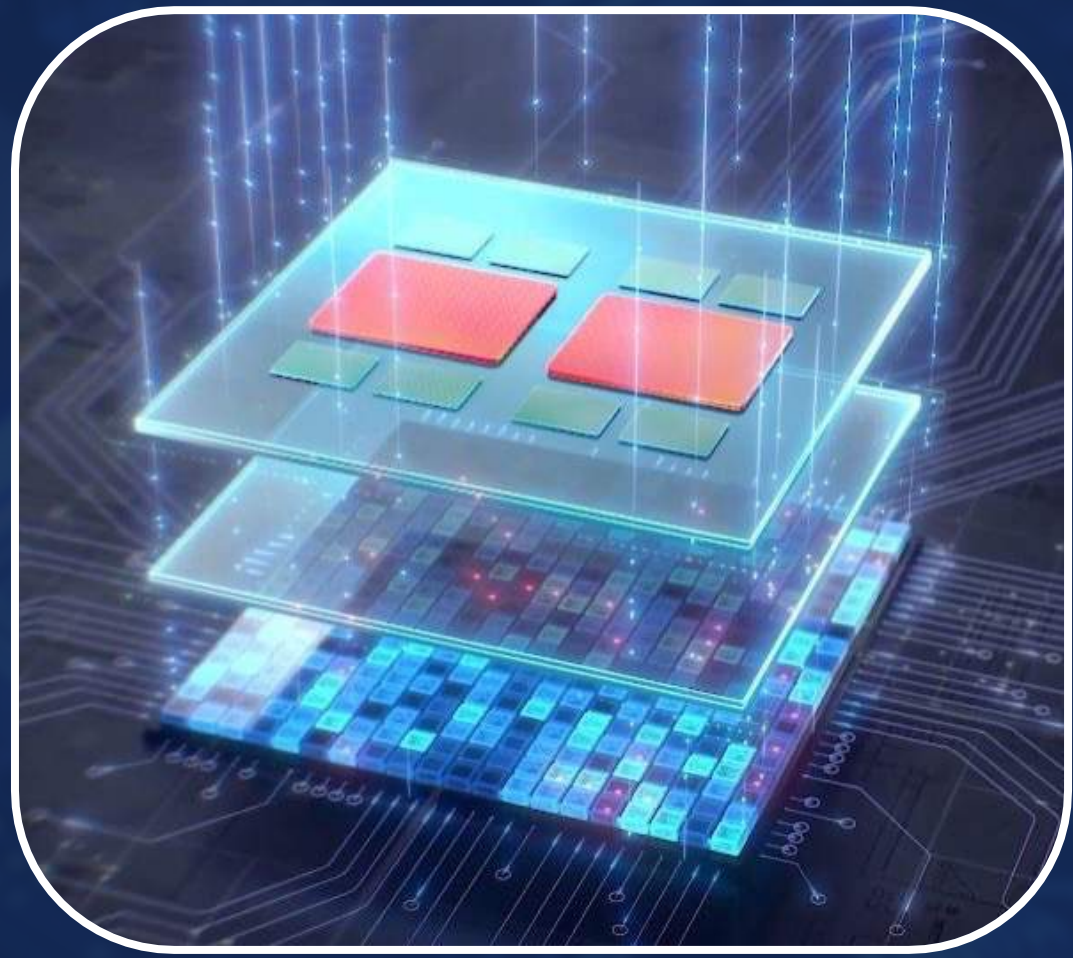
BEYOND MOORE'S LAW

As process innovation slows, design innovation needs to develop new techniques to achieve greater performance

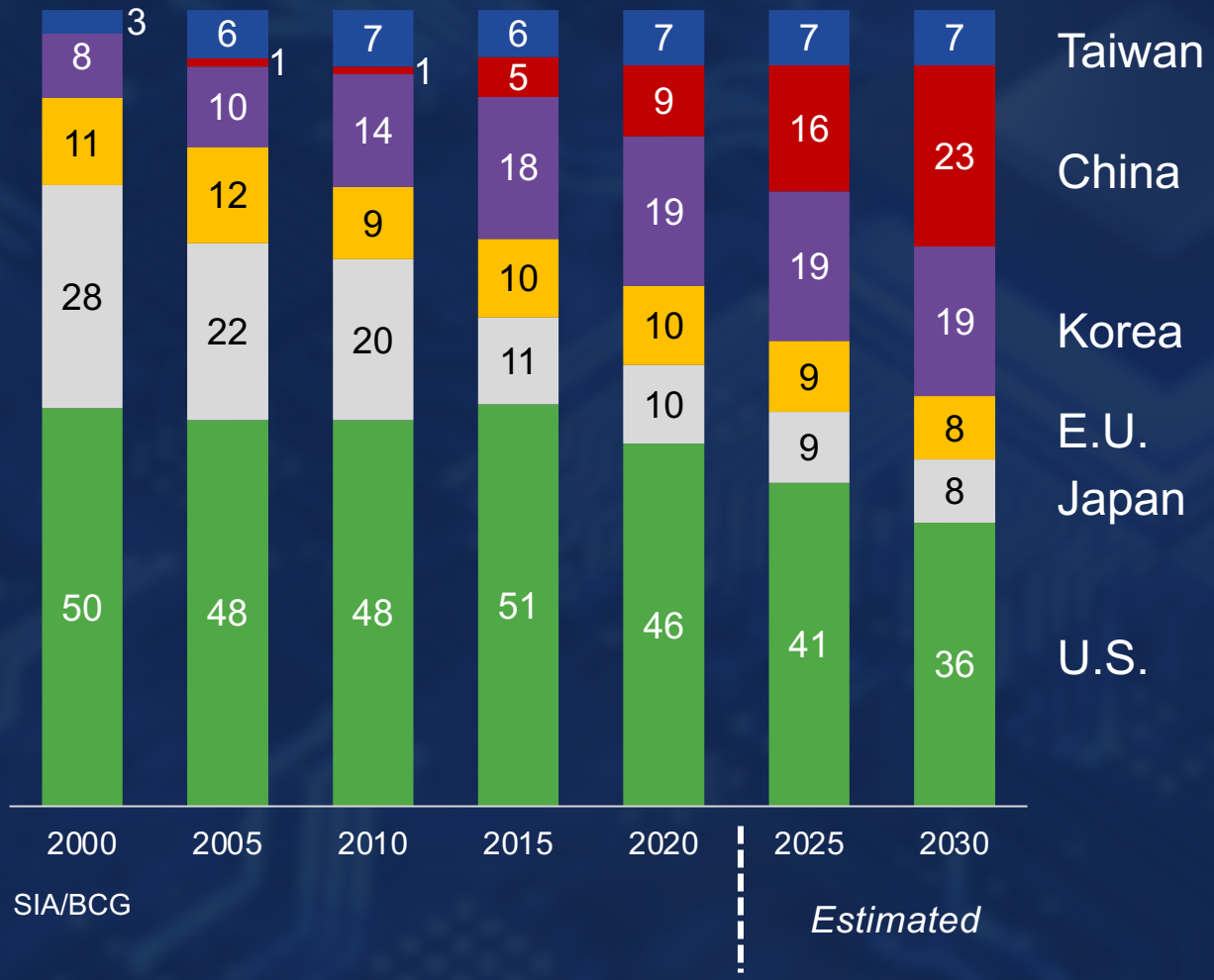
Design-driven innovation:

- Advanced packaging techniques (3D heterogeneous integration, stacking, chiplets, etc.)
- New materials
- Application specific integrated circuits and other domain-specific architectures
- Design tool improvement
- Design for security



CHALLENGES TO U.S. LEADERSHIP

U.S. Global Chip Revenue Market Share Projected to Fall to 36% by 2030; China Market Share Expected to Jump to 23%



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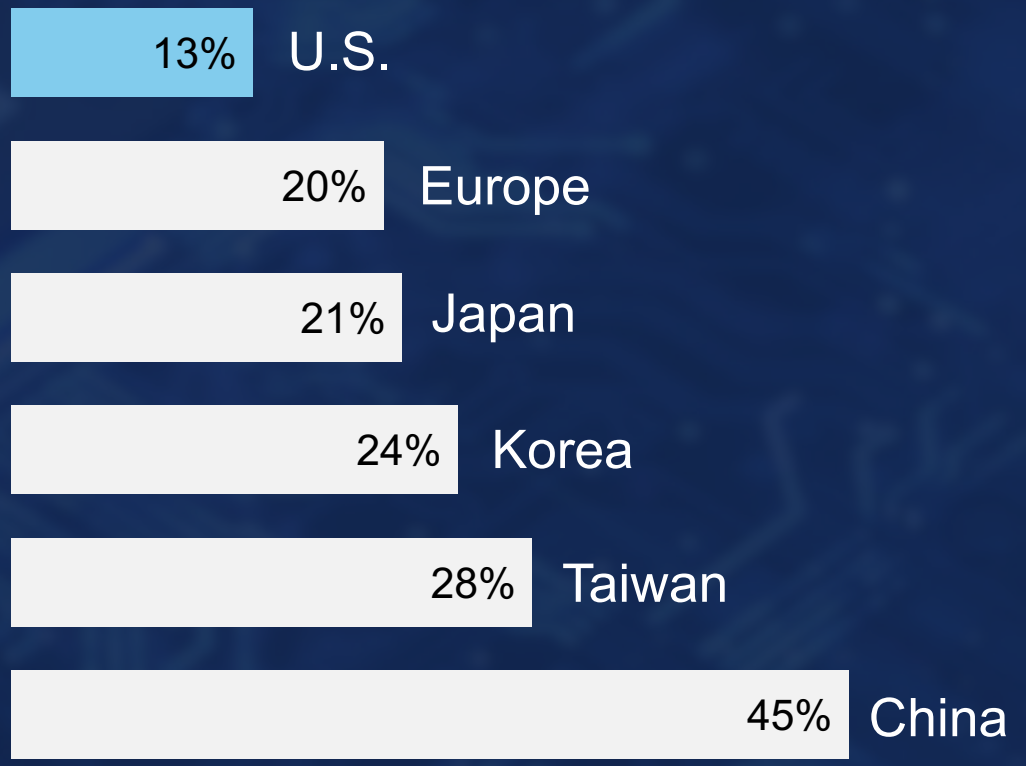
Estimated

Share of Semiconductor-Specific Design and R&D Funded by Public Investment



Source: OECD national accounts data and ITIF; WSTS data; SIA; BCG analysis

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GLOBAL INCENTIVES FOR CHIP DESIGN

CHINA

14th Five-Year Plan

National Integrated Circuit Investment Fund invests $3 billion in design

More than $30+ billion in additional state financing for R&D and other initiatives

Corporate income tax exemption for key design companies for 5 years after first profitable year; reduced tax rate of 10% after

Revamped stock market rules to establish STAR Market, on which fabless firms have raised over $50 billion through IPOs

TAIWAN

Taiwan Chips Act

25% R&D tax credit

Up to 200% credit for self-developed IP R&D expenditures

100% tax credit for foreign IP/licensing royalties

Up to 50% R&D grants for pre-competitive R&D and foreign R&D

$300 million over 7 years for semiconductor R&D

EUROPE

EU Chips Act

$12.6 billion in research, design, & innovation funding

EU-funded European Processor Initiative for design

Spain: $1.4 billion for chip design

KOREA

K-Belt Strategy

Up to 50% R&D tax credit

$1.3 billion over 10 years for AI & power chip design

Establish “Korean Fabless Valley” in Pangyo

JAPAN

Revitalization Strategy

$2.7 billion for R&D Consortium beyond 2nm

$750 million supercomputing design initiative

INDIA

Design Linked Incentive Scheme

Up to 50% design credit

Source: SIA analysis on data from gov’t semiconductor policies, company financial filings, news reports, EU R&D Scoreboard, SEMI World Fab Watch

WORKFORCE CHALLENGES

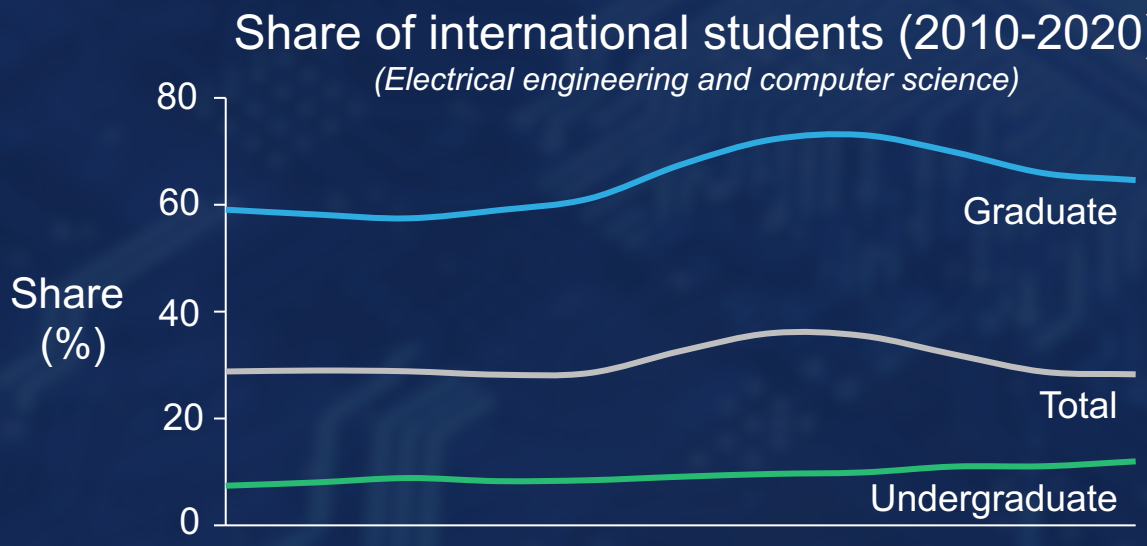
Note: SIA/Oxford Economics workforce report, forthcoming, will provide additional detail on STEM workforce

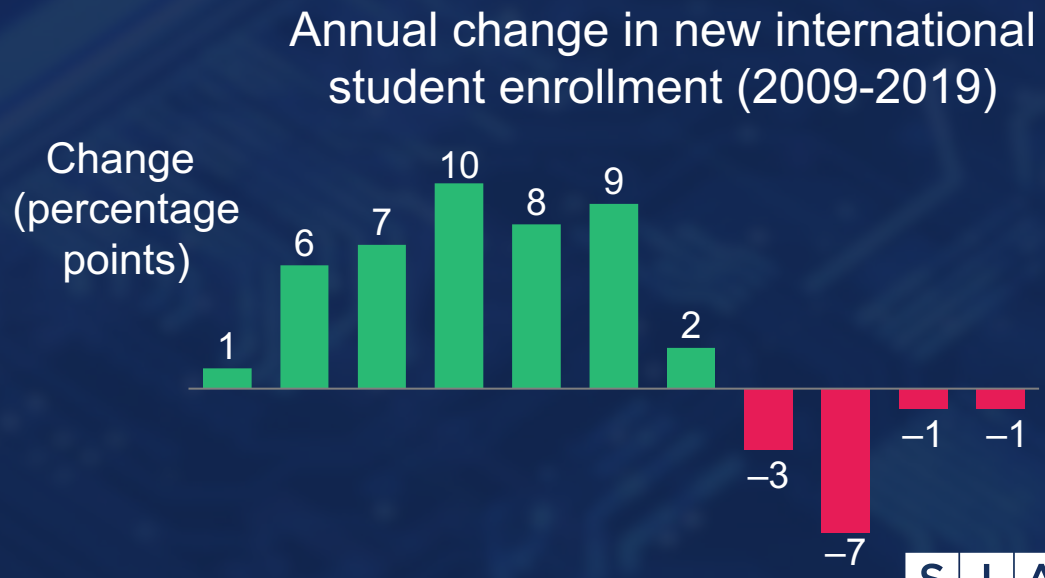
Existing and growing design talent shortage

Demand for U.S.-based design workers in 2030		Supply of U.S.-based design workers in 2030		Shortage of design workers in 2030
89,000	–	66,000	=	23,000

BA/MA = 90% *PhD = 10%*

Decreasing availability of international STEM talent, particularly MA/PhD





Sources: Shanghai Ranking; IIE, "New International Student Enrollment: International Student Data from the 2020 Open Doors Report."

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A POLICY AGENDA FOR 21st CENTURY U.S. CHIP DESIGN LEADERSHIP

Chip Design Investment Tax Credit

Incentivize chip design and strengthen the U.S. semiconductor ecosystem

Tax Policy to Promote, not Penalize, Innovation

Restore full deductibility of R&D expenditures and strengthen the R&D tax credit

Ensure Access to Foreign Talent

High-skilled immigration reform to attract global STEM talent and retain foreign STEM graduates of U.S. universities

Increase Investment in Research and STEM Education

Fully fund semiconductor research at federal agencies (NSF, NIST, DOE, DOD, EDA, etc.), and invest in the U.S. STEM talent pipeline from K-PhD

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THANK YOU

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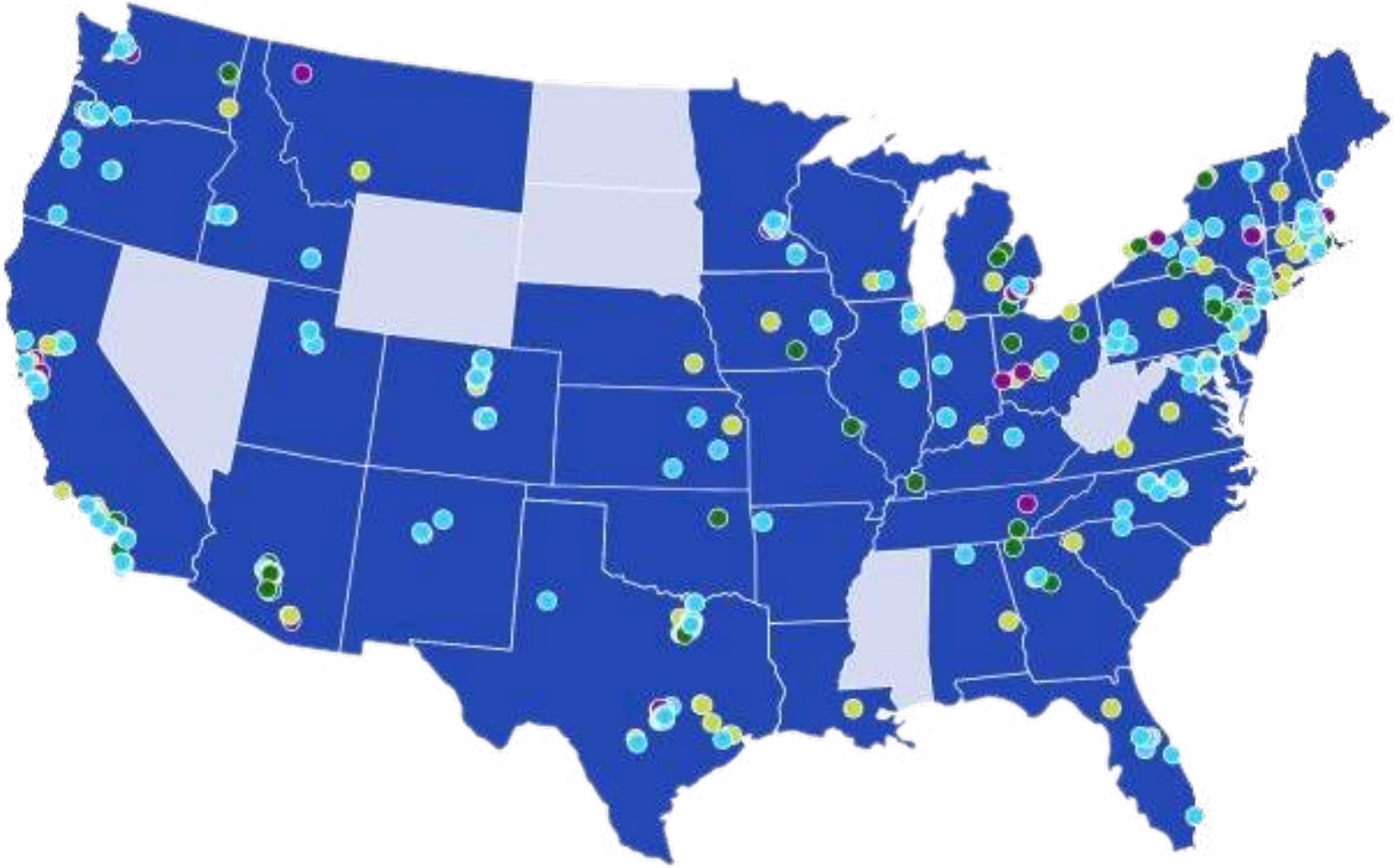
U.S. SEMICONDUCTOR ECOSYSTEM

Semiconductors Equipment Materials University R&D Partners



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U.S. CHIP DESIGN ECOSYSTEM